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Courant Institute of
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AEC Computing and Applied Mathematics Center

# An Interface Between a Control Data 6000 Series Computer and a Honeywell 16-Bit Series Computer

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# 1. INTRODUCTION

The basic design of an interface between an I/O channel of the Control Data 6000 series computers and the Honeywell 16-bit series computers is described in this report. The basic design incorporates an interaction of software and hardware techniques. The report includes a brief discussion of the I/O structure and instruction list of each computer and logic diagrams of the basic and implemented designs.

This interface makes possible the configuration in which a small computer is used as a front-end to a large central computer. Some salient features of this configuration are:

a. Each computer can operate independently (stand alone).

b. The small front-end computer becomes an universal programable I/O controller, not a hard wired one.

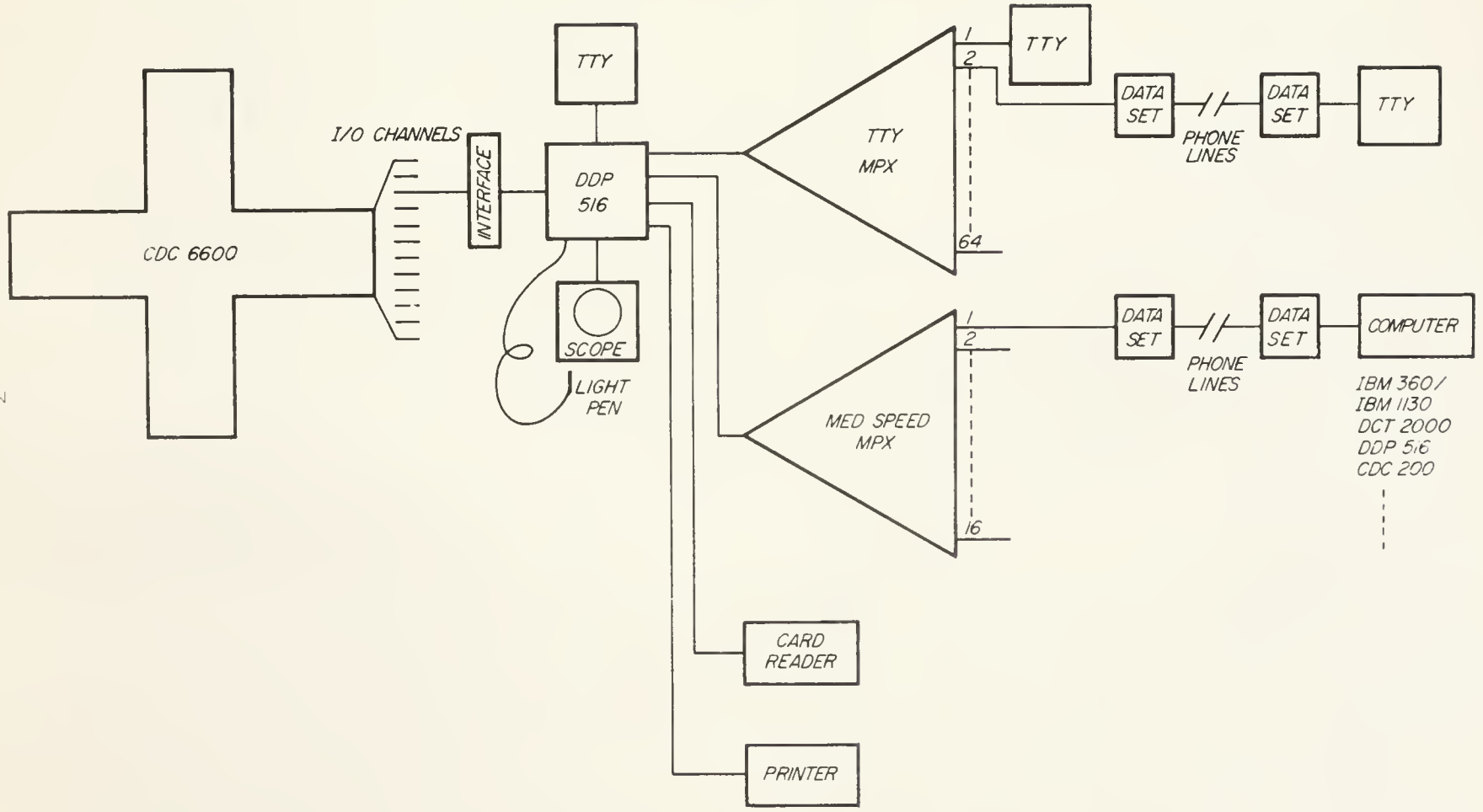
c. A more general high level I/O communications package between both computers can be designed.

d. Extensions or modifications to the I/O system become easy to implement and can be effected without halting operations — a necessity in a research environment.

e. The small computer liberates resources of the large central computer, i.e., PP computer time and channel time.

The interface described herein has been in use, during the past three years, in the interactive SHARER system and in the Remote Batch system at the AEC Computing Center at the Courant

Institute of Mathematical Sciences. A diagram of the configuration at the Computing Center appears on the next page. The interface is also employed in the development of graphic capabilities for both systems and as a tool for user-computer networks.




6600/516 CONFIGURATION

## 2. CONTROL DATA 6000 SERIES I/O CHANNEL

The 6000 series I/O channel contains two bundles of coax lines: one for input and the other for output.

The output bundle contains 19 coax leads:

12 - for data
1 - for function
1 - for active
1 - for inactive
1 - for full
1 - for empty
1 - for master clear
1 - for 10 MHz clock

The input bundle contains 15 coax leads:

12 - for data
1 - for inactive
1 - for full
1 - for empty

Signals on the output coax leads are AC pulses: 35 nanoseconds wide, and 1 volt in amplitude.

Signals on the input coax leads are AC pulses: 35 nanoseconds wide, 1 volt in amplitude, and synchronized with the 10 MHz clock. The synchronization requirement was found to be unnecessary if a 50 nanosecond "dead time" out of 1000 nanoseconds is avoided, or if multiple word inputs and outputs are not used. This latter solution yields many advantages. From a hardware point of view, the synchronization of the channel with the 10 MHz

clock is not required. From a software point of view, an interface can be programed so that it cannot "hang" the system.

The I/O software instructions and their hardware significance are discussed briefly. On 6000 series machines, I/O commands are executed with peripheral processors (PP's). The 6000 series I/O channels have no hardware interrupt facility; instead, demand of I/O devices must be satisfied by a software scan.

Activate Channel n (ACN)

An activate instruction sends out a single pulse on the active output coax lead of the selected channel. This signals the device that data flow will follow.

Disconnect Channel n (DCN)

A disconnect instruction sends out a single pulse on the inactive output coax lead of the selected channel. This signals the device that data flow has stopped.

Function Channel n (FAN or FNC)

This instruction is issued on an inactive channel, and when issued successfully, an inactive signal is returned by the I/O interface. When a function instruction is issued, a 12-bit word is placed on the 12 output coax data leads in coincidence with a pulse on the function lead. This 12-bit word addresses an interface and gives it a command. The addressed interface accepts the 12-bit word, and returns an inactive pulse on the input inactive coax lead.

This instruction is issued to control the data flow in an interface.

Output on Channel n (OAN or OAM)

Output instructions are issued on an active empty channel. Single word output and multiple word outputs are similar in hardware operation. A 12-bit word is placed on the 12 output coax data leads in coincidence with a pulse on the output full lead. When accepted, an empty pulse is returned on the input empty coax lead. On the single word output (OAN), the output full pulse completes the issued instruction. On multiple word outputs (OAM), the returned empty must be synchronized with the 10 MHz clock. This returned empty triggers the next output until all outputs are accepted. Then the (OAM) instruction is completed.

Input on Channel n (IAN or IAM)

Input instructions are issued on an active channel. When issued, 12-bits from the 12 input data coax leads, in coincidence with or delayed from a pulse on the input full lead, are accepted as input. A pulse on the output empty lead is sent as an acknowledgement of this input. On the single word input (IAN), the pulse on the output empty lead completes the instruction. On multiple word inputs (IAM), the 12 input pulses and the input full pulse must be synchronized with the 10 MHz clock. The empty acknowledgement will continue until all input words are accepted. Then the (IAM) instruction is completed.

The following instructions have only software significance in that they test conditions of the channel.

Active Jump on Channel n (AJM)

This instruction when issued causes a jump to a routine when channel n is active.

Inactive Jump on Channel n (IJM)

This instruction when issued causes a jump to a routine when channel n is inactive.

Full Jump on Channel n (FJM)

This instruction when issued causes a jump to a routine when channel n is full.

Empty Jump on Channel n (EJM)

This instruction when issued causes a jump to a routine when channel n is empty.

If the Full Jump instruction is used with the single word input instruction, and the Empty Jump instruction is used with the single word output instruction, then the 6000 series channel can be used completely asynchronously. These instructions coupled with software timers can avoid "hung" channels or "hung" peripheral processors (PP's). The rate of multiple word transfers accomplished by a loop that incorporates the single word transfer instruction (IAN or OAN) with the jump instruction (FJM or EJM) is one 12-bit word per 10 microseconds. The rate of multiple word transfers accomplished by the multiple word transfer instruction (IAM or OAM) is one 12-bit word per microsecond.

Refer to Control Data's Input-Output Specifications (Pub. No. 60045100) for further details on the 6000 series I/O channel.

## 3. HONEYWELL 16-BIT SERIES STANDARD I/O CHANNEL

The Honeywell 16-bit series standard I/O channel is a shared bus I/O system that consists basically of 48 twisted lead pairs. Thirty pairs are used for output and 18 pairs for input.

The 30 output twisted lead pairs are:

16 - for data bits (OTBXX)
10 - for address (ADBXX)
1 - for reset ready (RRL)
1 - for output command (OCP)
1 - for master clear (MSTCL)
1 - for set mask (SMSK)

The 18 input twisted lead pairs are:

16 - for data bits (INBXX)
1 - for device ready (DRL)
1 - for program interrupt (PIL)

Signals on the output and input leads are DC levels: 0 or -6 volts in the DDP-116 and 0 or +6 volts in the DDP-416, DDP-516, and H-316. All leads are shared with all interfaces. Memory Access I/O channels are available as options for all these 16-bit computers.

The channel is synchronized by a specific time sequence of events. For example, within any of the I/O instructions there exists the following sequence of events: (a) an address goes out on the address bus, (b) a device decodes this address and responds, and (c) a strobe for the device terminates the instruction. The standard channel provides a hardware program interrupt

feature to service devices on demand. The standard channel is a parallel I/O bus that is shared by all interfaces under program control.

The I/O software instructions and their hardware significance are discussed briefly.

Output Command (OCP)

This instruction initiates DC levels on the 10-bit address bus and a delayed pulse on the output command twisted pair. This instruction is used to control the functioning of the I/O device, and expects no response from the device.

Sense Condition (SKS)

This instruction initiates DC levels on the 10-bit address bus and senses the input device ready lead. When a signal appears on this lead, during a set time in the instruction period, it causes the next instruction to be skipped. If no signal appears, the next instruction will be executed. This (SKS) instruction is used to test conditions of specific interfaces on the I/O bus.

Single Word Input (INA)

The input instruction initiates action by placing DC levels on the 10-bit address bus. The addressed interface then places its input data on the 16-bit input bus; simultaneously, a signal is placed on the input device ready lead. The computer will acknowledge the input with a signal on the output reset ready lead, and will skip the next instruction to be executed. In the event of no input, the addressed interface does not return a device ready

signal. The computer does not skip the next instruction, nor acknowledge an input with a signal on the reset ready lead. Multiple word inputs must be accomplished by creating a program loop of single word (INA) inputs.

Single Word Output (ØTA)

The output instruction initiates action by placing DC levels on the 10-bit address bus and the 16-bit output bus. The addressed interface accepts the data by placing a signal on the input device ready lead. The computer will then respond on the reset ready lead with a signal which can be used as a strobe for the output data. The computer will then skip the next instruction to be executed. In the event in which the addressed interface does not accept the output, the computer will not skip the next instruction, nor respond with a signal on the reset ready lead. Multiple word outputs must be accomplished by creating a program loop of single word (ØTA) outputs.

Any interface on the I/O bus can initiate an interrupt by placing a DC level on the program interrupt lead (PIL). Since this lead is common to all interfaces, when an interrupt occurs a program using the sense condition instruction (SKS) must be used to seek out the source of interrupt, and then jump to a subroutine to service it. Priorities of program interrupts are accomplished through the use of mask bits. Each interface is assigned a bit which is used to generate its program interrupt (PIL) signal.

Refer to Honeywell Interface Manual (Pub. No. 130071624) for further details on the I/O channel of the 16-bit series computers.

# 4. BASIC INTERFACE DESIGN

The basic design discussed here is one between a Control Data 6600 and a Honeywell DDP-516. The design is applicable to any of the Control Data 6000 series computers and any of the Honeywell 16-bit machines (DDP-116, DDP-416, DDP-516, H-316). In the discussion, however, the machines will be referred to as the 6600 and 516.

The interface between the 6600 and 516 acts as a transmission channel between the two machines, wherein compatibility is obtained in word size and signal form (AC pulse versus DC level). Even more important, however, is the designed capability of the interface to arrange communication between the two computers: messages from one computer to the other are "placed" on the interface (written into a register), where they can be read by each computer at its own convenience.

## A. HARDWARE STRUCTURE

The interface hardware contains 28 flip-flops with associated "nand gate" logic. Pulse amplifiers and pulse stretchers are employed as transmitters and receivers for the 6600 I/O channel. The flip-flops are distributed among a Status Register, a Holding Register, and Control Circuits.

Status Register

The Status Register is 12-bits in length and is used to store messages for both computers. The register can be read by both machines. The individual bits of the register have this significance:

6600 bits

4-bits written by the 6600 are for software control.
1-bit written by the 6600 is for direction of data flow through the interface (Direction Bit).

Shared bits

1-bit is set by the 6600 to interrupt the 516, and is reset by the 6600 or the 516 (Interrupt Bit).
1-bit is set by the 6600 and reset by the 516 (Ping Pong Bit).

516 bits

1-bit written by the 516 is for interrupt priority (Mask Bit).
4-bits written by the 516 are for software control.

As can be seen by this list, some bits of the Status Register have hardware significance, and they control aspects of communication between the computers; other bits are used in program control as desired. Note that 5-bits are 6600 bits, 2-bits are shared, and 5-bits are 516 bits.

Holding Register

Data flows between the 6600 and 516 in 12-bit words. A 12-bit Holding Register is used in the interface to staticize the 12 data bits from the 6600 to the 516. The 12 data bits from the 516 to the 6600 are staticized with a 12-bit register in the 6600. In other words, transmission from the 6600 to the 516 passes through a 12-bit Holding Register in the interface, but the 516 outputs 12-bit data directly through the interface to the 6600.

Control Circuits

Aside from the Direction Bit, Interrupt Bit, and Mask Bit, the Control Circuits employ 4 other bits for the flow of signals in the interface. The 4 other bits are: Active, Connect, Full and Status Read. The Active and Full flip-flops are duplicates of the Active and Full conditions of the 6600 I/O channel. The Connect flip-flop will be set only when the I/O channel has selected this interface for communications. The Status Read flip-flop will be set when the 6600 requests status, and will, in turn, set up controls for subsequent transmission of the Status Register to the 6600 when the I/O channel goes Active. The rest of the Control Circuits employ 516 "nand gate" logic for setting up transmission and for answering the control lines of both computers.

Pulse Amplifiers and Pulse Stretchers

Pulse amplifiers and pulse stretchers, incorporated in the interface, terminate the 6600 I/O channel and translate logic levels. The 35 nanosecond, 1 volt, AC pulses from the 6600 output cables are converted by the pulse stretchers to 100 nanosecond,

0 and +6 volts, DC pulses. Conversely, the 100 nanosecond, 0 and +6 volts, DC pulses are converted by the pulse amplifiers to 35 nanosecond, 1 volt, AC pulses required by the 6600 input cables. Since the interface is designed with 516 type logic, level changers for the 516 I/O bus are not required.

## B. SOFTWARE STRUCTURE

The designed software structure provides a generalized I/O communications routine that utilizes the existing 6600 operating system with minor modifications. Also incorporated in the structure is an implemented modular 516 software package. This package facilitates modification or expansion of future systems.

The 516 front-end computer appears to the 6600 operating system as one device with many buffers. The number of buffers is a software parameter. A 516 I/O device is assigned to each buffer. The detailed status of these buffers are also software parameters, and are transferred during computer communications. The Status Register is utilized to initiate communications when data in the buffers are ready for transfer. Data transmitted through the interface are in blocks of variable length. The interface is completely transparent to the actual data transmission.

The hardware structure of the two computers (one interruptable, the other not) requires that one machine take the initiative for establishing communications. For example, the 516 requests service of the 6600 by setting bits of the Status

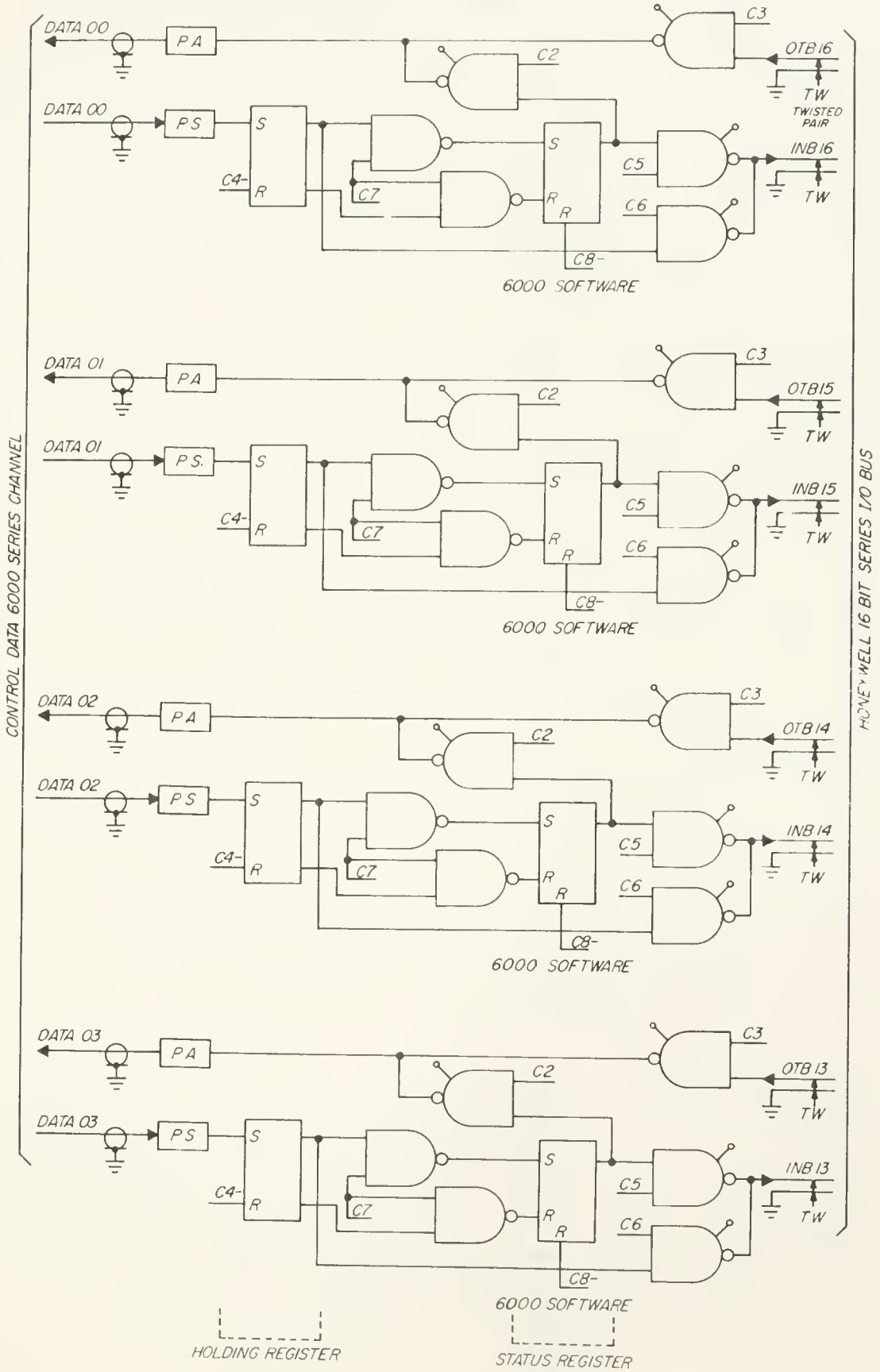
Register. The 6600 must be programed to read periodically the Status Register and upon finding a request, proceed to write a status that includes the setting of the 516 Interrupt Bit. When the 516 interrupt is acknowledged, both machines exchange the detailed parameters of the data in the buffers to be transferred. Then upon agreement proceed to transfer the data. Upon completion of the data transfer, both machines return to their respective main programs, and await further communication action. The Ping Pong bit of the Status Register is utilized by the software to synchronize communications between the two machines.

An important feature of the implemented software structure is its ability to abort and recover communications in the case of excessive delays. These delays can be caused by higher priority interrupts of the 516, or by hardware or software failure. The 516 software was implemented using an extremely modular executive program (EXEC) which contains many subprograms, one of which handles the 6600 communications. This (EXEC) software also provides means of communication with 516 devices on a "Stand Alone" basis. The 6600 I/O software contains two PP overlay routines: one for output (2LR) and the other for input (2RR). Both routines are called by the system's general purpose I/O routine (CIO). One way of initiating the 6600 I/O routine (CIO) is with Fortran Read or Write Statements. Utilizing this facility, the 516 buffers can be read or written with Fortran Statements. Furthermore, several Fortran programs can operate simultaneously on the 6600 utilizing different, or the same, 516 buffers. The 516 is, therefore, a device which can be shared by different programs running concurrently in the 6600.

## C. LOGIC DIAGRAMS

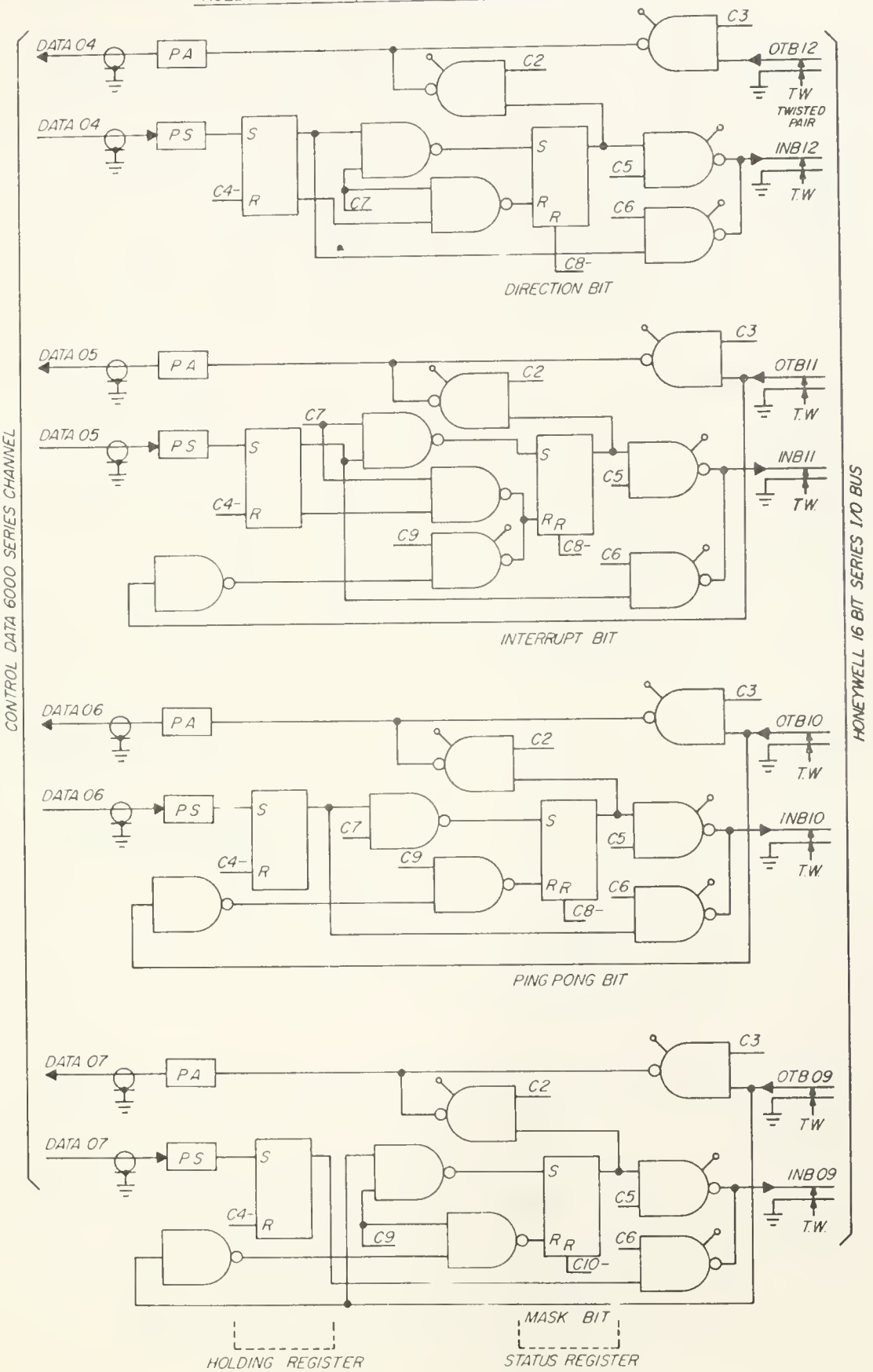
BASIC INTERFACE DESIGN

HOLDING REGISTER, STATUS REGISTER AND DATA FLOW



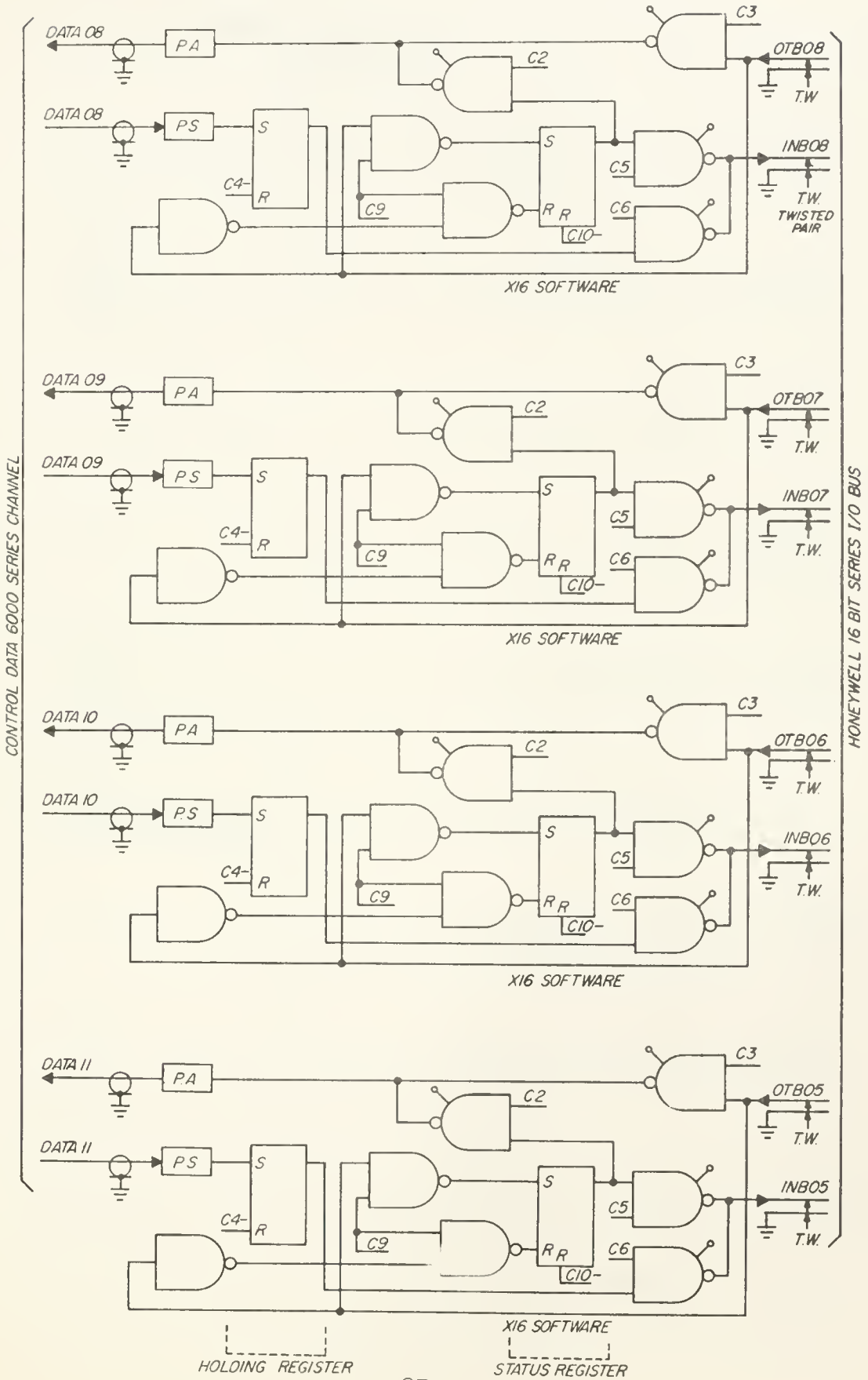
BASIC INTERFACE DESIGN

HOLDING REGISTER, STATUS REGISTER AND DATA FLOW



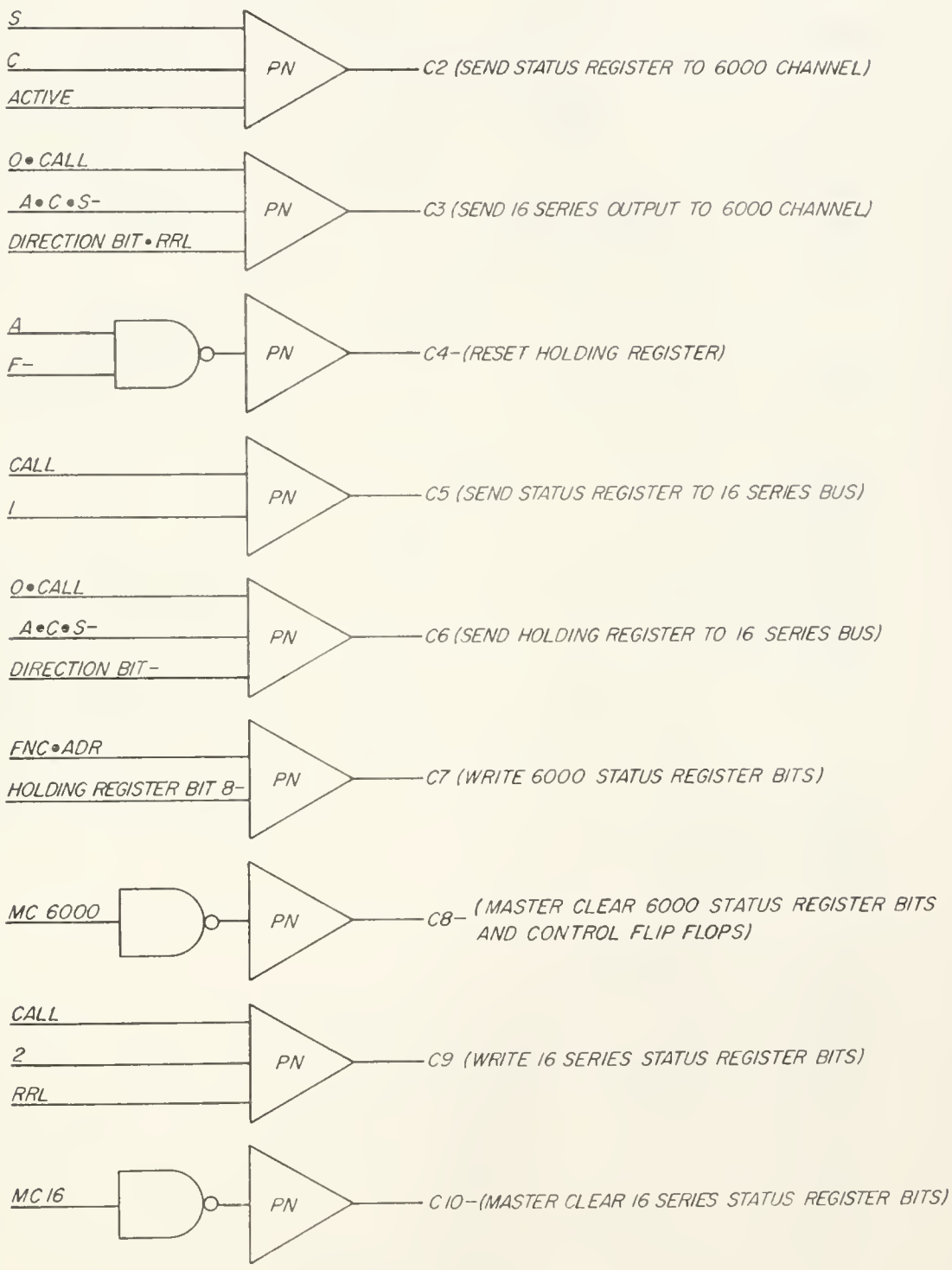
BASIC INTERFACE DESIGN

HOLDING REGISTER, STATUS REGISTER AND DATA FLOW



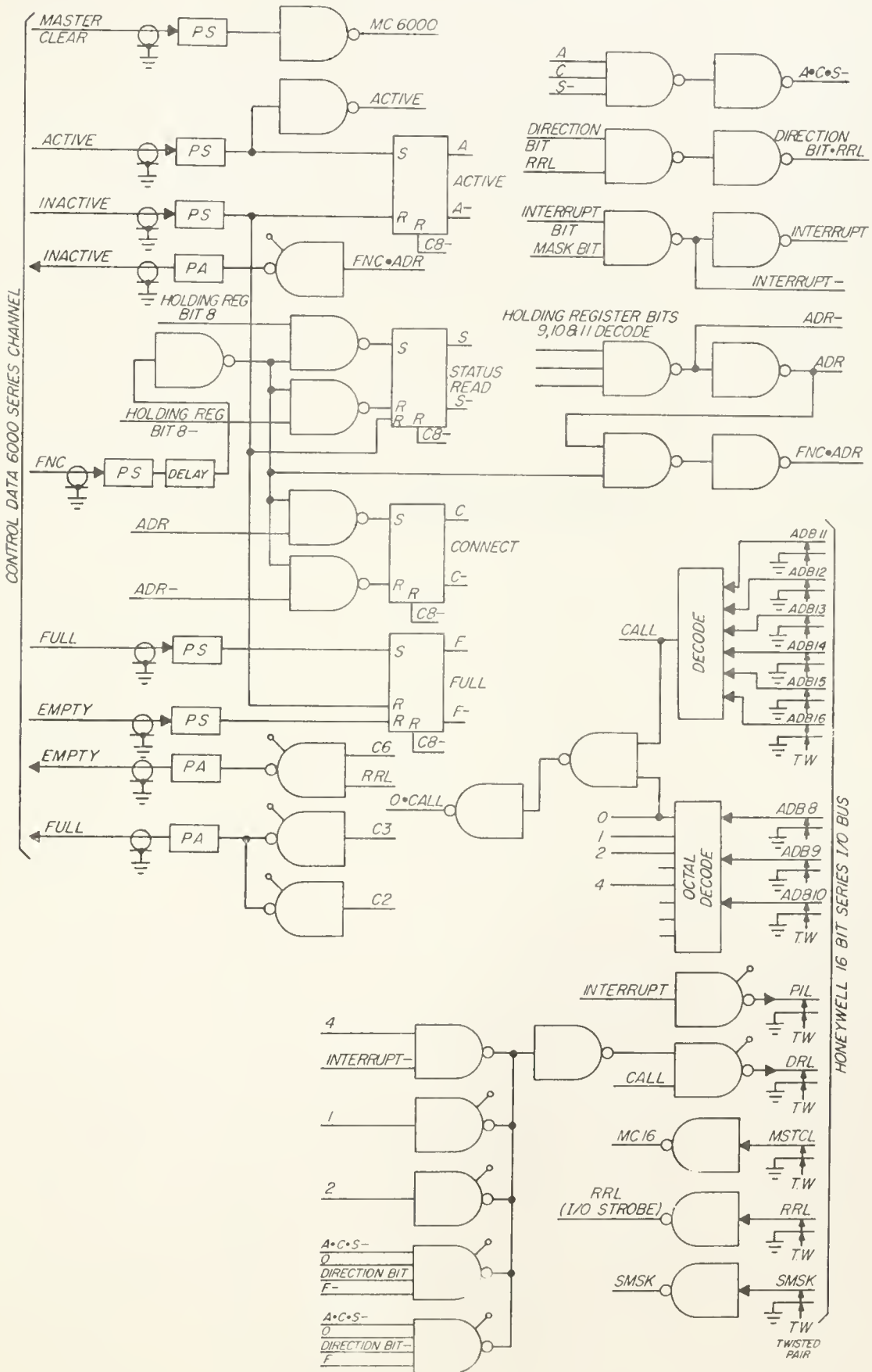
BASIC INTERFACE DESIGN

CONTROL CIRCUITS

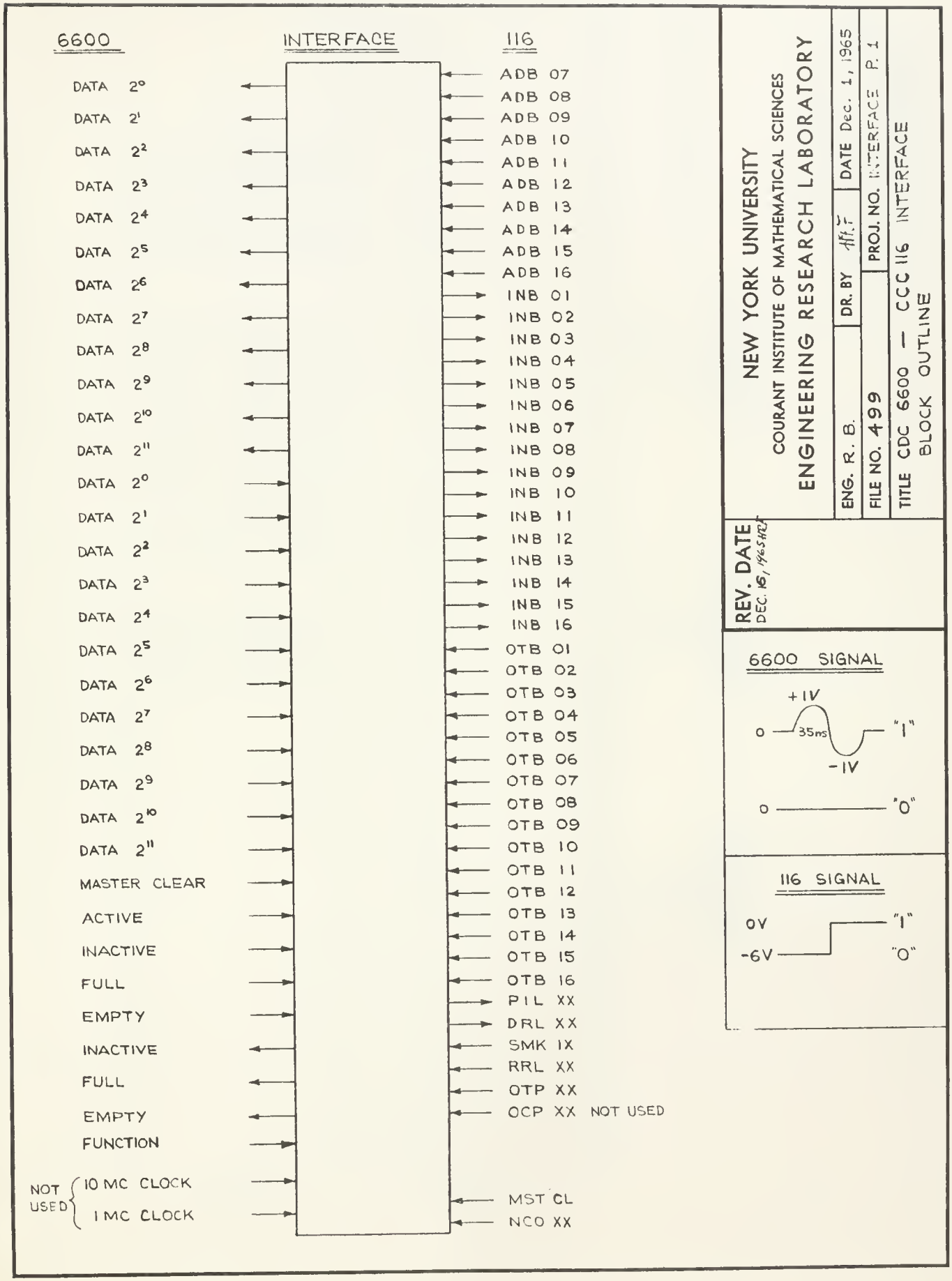



PN'S ARE POWER DRIVE "AND" GATES

## CONTROL CIRCUITS AND CONTROL FLIP FLOPS



# 5. IMPLEMENTED INTERFACE SCHEMATICS


6600
INTERFACE
116
DATA 2^0
DATA 2^1
DATA 2^2
DATA 2^3
DATA 2^4
DATA 2^5
DATA 2^6
DATA 2^7
DATA 2^8
DATA 2^9
DATA 2^10
DATA 2^11
DATA 2^0
DATA 2^1
DATA 2^2
DATA 2^3
DATA 2^4
DATA 2^5
DATA 2^6
DATA 2^7
DATA 2^8
DATA 2^9
DATA 2^10
DATA 2^11
MASTER CLEAR
ACTIVE
INACTIVE
FULL
EMPTY
INACTIVE
FULL
EMPTY
FUNCTION
NOT USED
10 MC CLOCK
1 MC CLOCK
ADB 07
ADB 08
ADB 09
ADB 10
ADB 11
ADB 12
ADB 13
ADB 14
ADB 15
ADB 16
INB 01
INB 02
INB 03
INB 04
INB 05
INB 06
INB 07
INB 08
INB 09
INB 10
INB 11
INB 12
INB 13
INB 14
INB 15
INB 16
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OTB 04
OTB 05
OTB 06
OTB 07
OTB 08
OTB 09
OTB 10
OTB 11
OTB 12
OTB 13
OTB 14
OTB 15
OTB 16
PIL XX
DRL XX
SMK IX
RRL XX
OTP XX
OCP XX NOT USED
MST CL
NCO XX
NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
ENG. R. B.
DR. BY
DATE Dec. 1, 1965
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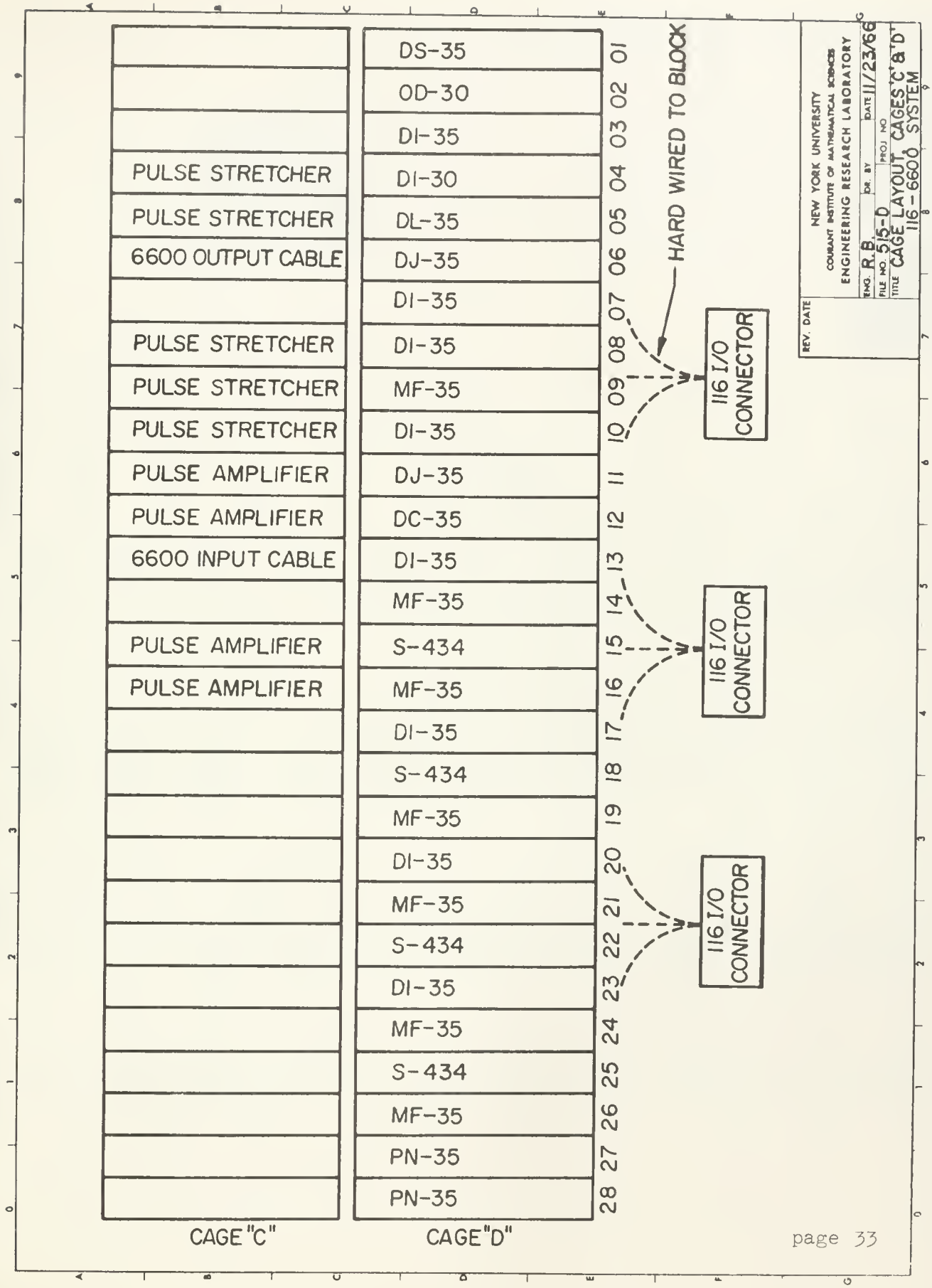
+1V
0
35ns
"1"
-1V
0
"0"
116 SIGNAL
0V
"1"
-6V
"0"
OGILVIE PRESS, INC., BROOKLYN 17, N. Y. CURRENCY NO. 140M 10067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CAGE "D"
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OD-30
DI-35
DI-30
DL-35
DJ-35
DI-35
DI-35
MF-35
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DJ-35
DC-35
DI-35
MF-35
S-434
MF-35
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S-434
DI-35
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PN-35
PN-35
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
PULSE STRETCHER
PULSE STRETCHER
6600 OUTPUT CABLE
PULSE STRETCHER
PULSE STRETCHER
PULSE STRETCHER
PULSE AMPLIFIER
PULSE AMPLIFIER
6600 INPUT CABLE
PULSE AMPLIFIER
PULSE AMPLIFIER
HARD WIRED TO BLOCK
116 I/O CONNECTOR
116 I/O CONNECTOR
116 I/O CONNECTOR
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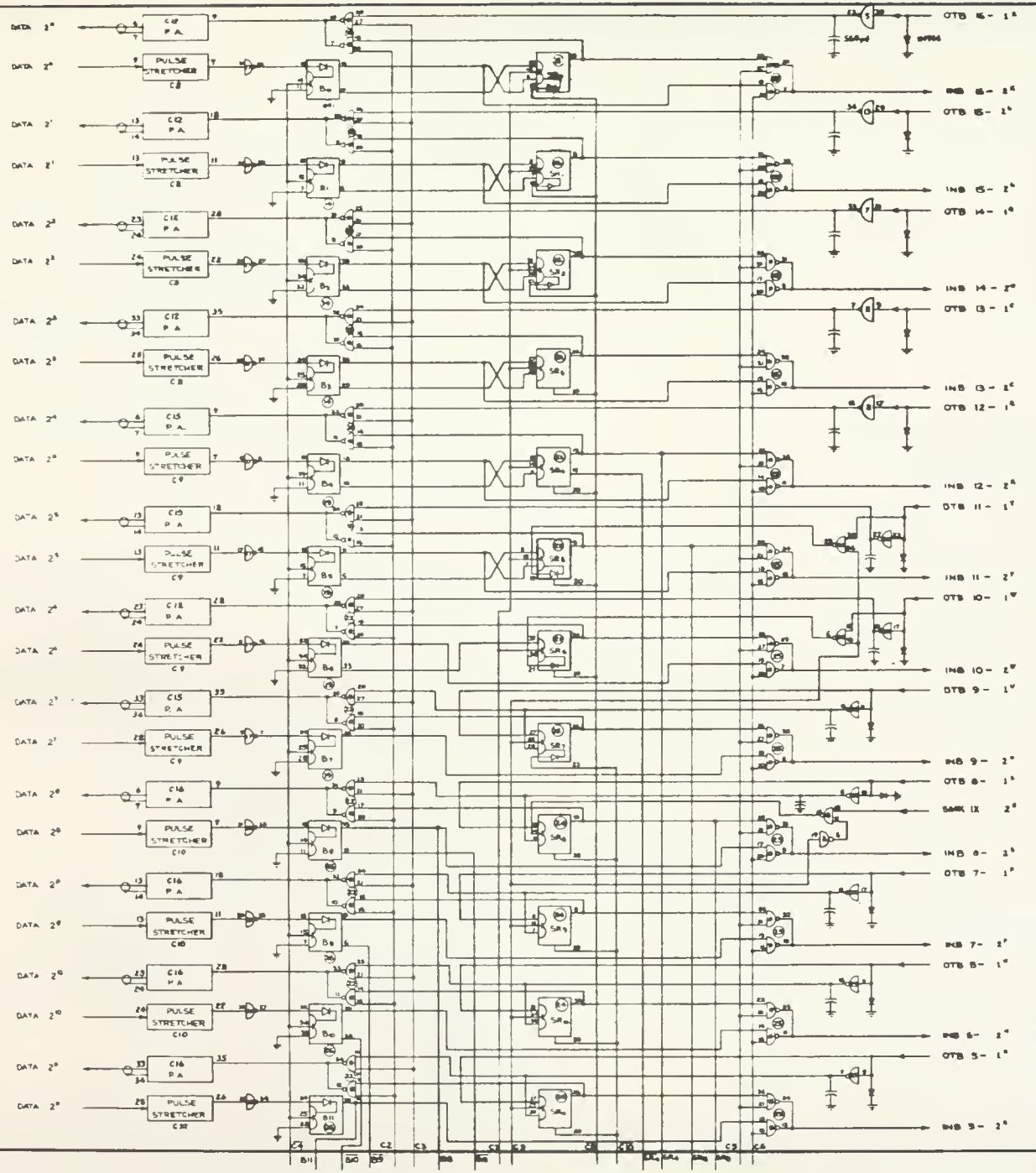
116-6600 SYSTEM
REV. DATE

page 33




NOTE:

I.
- C2- TRANSMIT DATA TO 6600
- C3- TRANSMIT S.R. TO 6600
- C4- CLEAR 6600 BUFFER REG.
- C5- ENABLE S.R. TO 116
- C6- ENABLE DATA TO 116
- C7- WRITE STATUS FROM 6600
- C8- MASTER CLEAR FROM 6600
- C9- WRITE STATUS FROM 116
- C10- MASTER CLEAR FROM 116

II. Ø REMOVE COLLECTOR LOAD RESISTOR.

III. NUMBERS CIRCLED Ø OR IN GATES ⑩ INDICATE CARD NUMBER IN CAGE "0"

IV DIODES - 1N914
CAPACITORS - 560 pf

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| | COURANT INSTITUTE OF MATHEMATICAL SCIENCES |
| | ENGINEERING RESEARCH LABORATORY |
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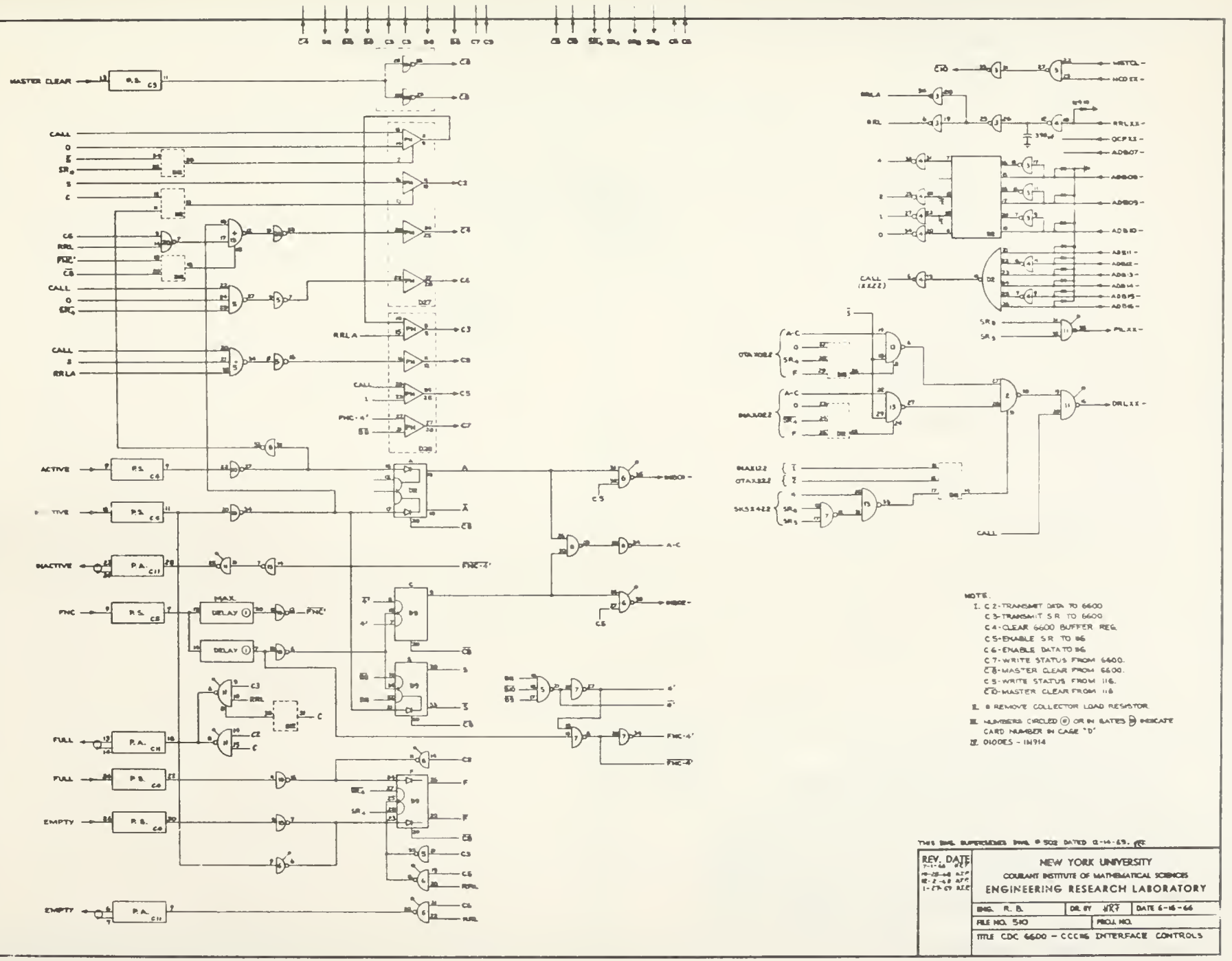
MASTER CLEAR
CALL
ACTIVE
INACTIVE
FNC
FULL
EMPTY
MAX. DELAY
DELAY
NOTE.
I. C2-TRANSMIT DATA TO 6600
C3-TRANSMIT S R TO 6600
C4-CLEAR 6600 BUFFER REG.
C5-ENABLE S R TO 116
C6-ENABLE DATA TO 116
C7-WRITE STATUS FROM 6600.
C8-MASTER CLEAR FROM 6600.
C9-WRITE STATUS FROM 116.
C10-MASTER CLEAR FROM 116
II. 8 REMOVE COLLECTOR LOAD RESISTOR.
III. NUMBERS CIRCLED ⓔ OR IN BATES ⓑ INDICATE CARD NUMBER IN CAGE "D"
IV. DIODES - 1N914
THIS ENG. SUPERSEDES ENG. # 502 DATED 12-16-65.
REV. DATE
7-1-66 RFF
10-28-66 AJP
12-2-66 AJP
1-27-67 AJP
NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
ENG. R. B.
DR. BY WRF
DATE 6-16-66
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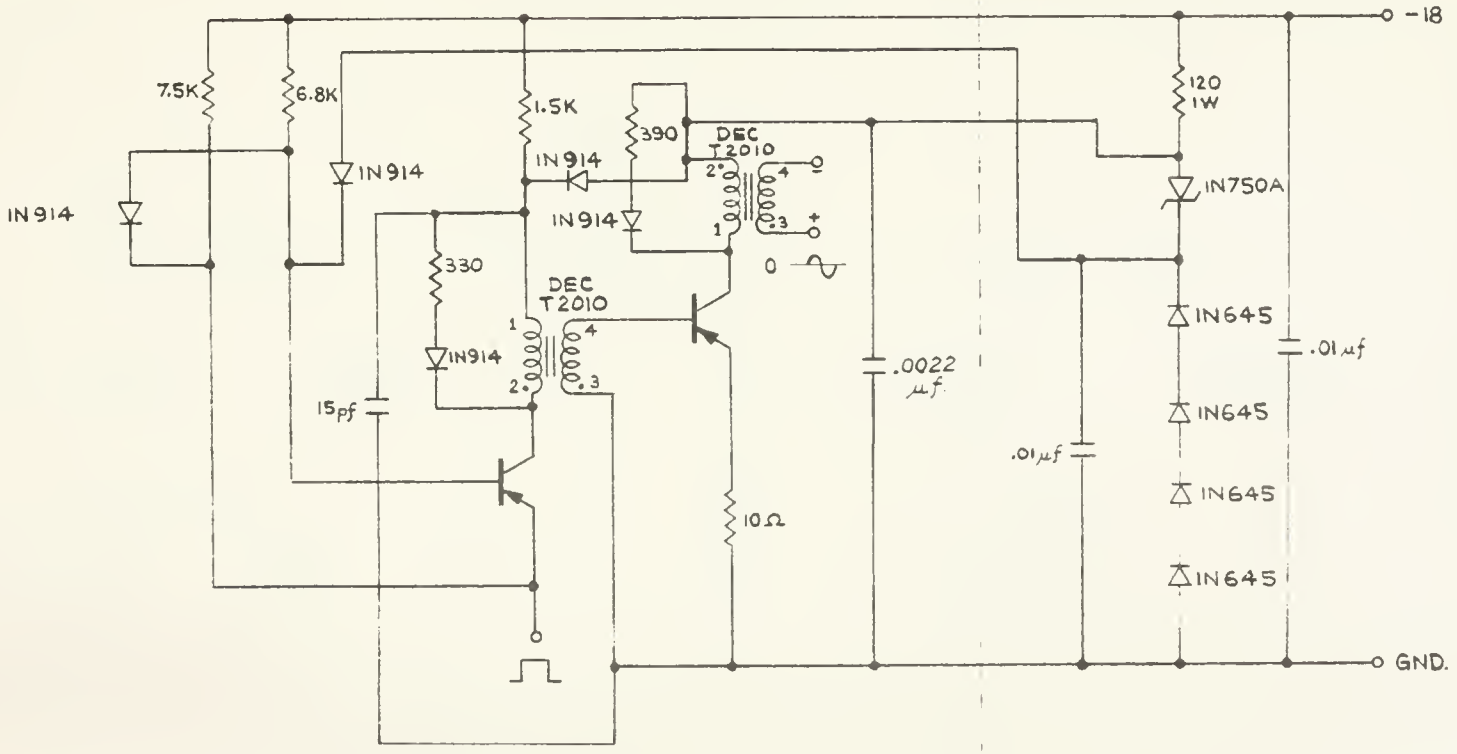
POWER SUPPLY COMMON TO ALL CIRCUITS.

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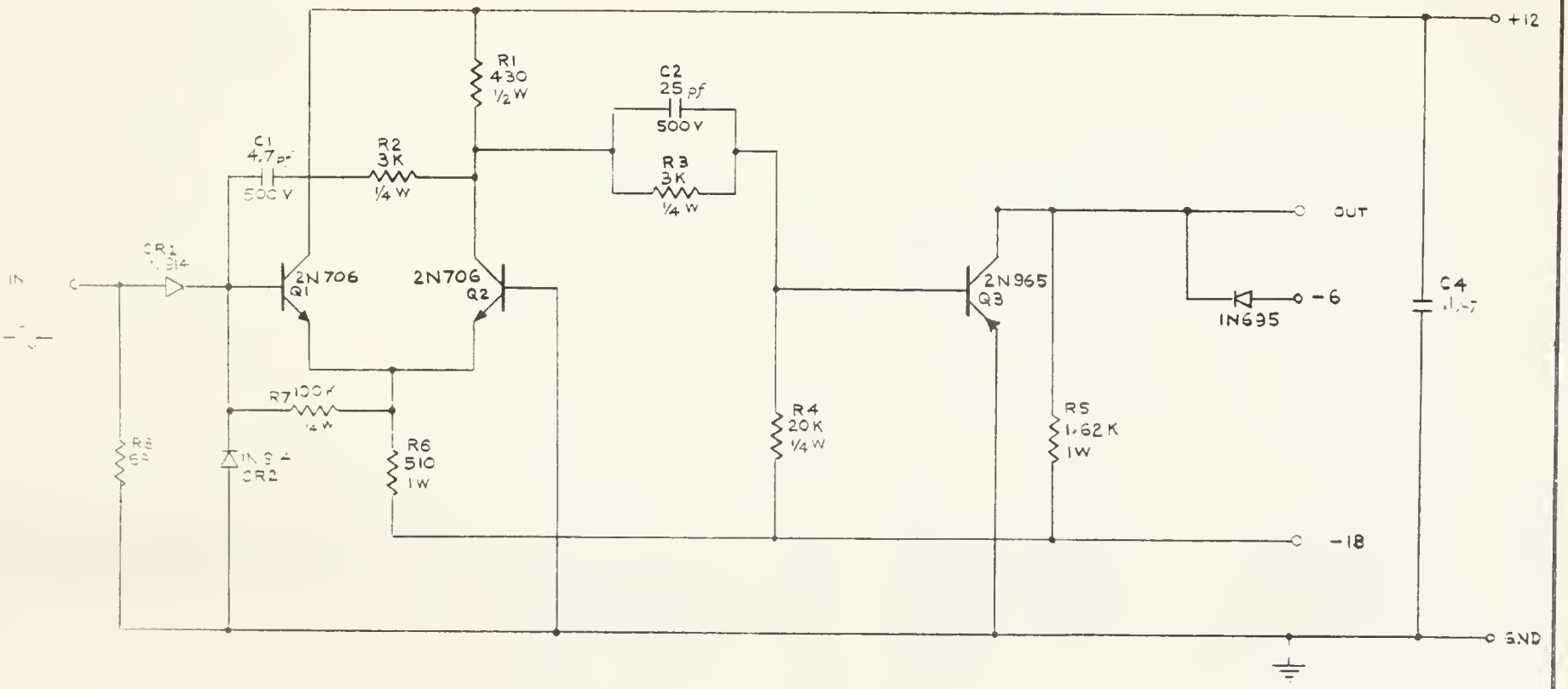


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